LISTING OF THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of the claims in this application:

Claim 1 (Currently Amended) A hybrid substrate comprising:

a first region having an upper surface of a second crystallographic orientation comprising a bottom semiconductor layer having a first crystallographic orientation which is different from said second crystallographic orientation and a top semiconductor layer having said second crystallographic orientation, wherein said top and bottom; ~~and~~

~~a second semiconductor layer having a second crystallographic orientation which is different from the first crystallographic orientation, wherein said first and second~~ semiconductor layers are vertically separated from each other by ~~an~~ a bonding interface, said ~~second~~ top semiconductor layer has a thickness from about 200 nm to about 2 μm and said interface has an oxide thickness of about 10 nm or greater; and

a second region having an upper surface of said first crystallographic orientation which is substantially coplanar with said upper surface of said first region, wherein said second region is absent of said bonding interface and comprises said bottom semiconductor layer and an epitaxial semiconductor layer.

Claim 2 (Currently Amended) The hybrid substrate of Claim 1 wherein said ~~first~~ bottom semiconductor layer and the ~~second~~ top semiconductor layer are composed of the same or different semiconductor material selected from the group consisting of Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, other III/V or II/VI compound semiconductors and any combination thereof.

Claim 3 (Currently Amended) The hybrid substrate of Claim 1 wherein said ~~first~~ bottom semiconductor layer and the ~~second~~ top semiconductor layer are both composed of Si.

Claim 4 (Currently Amended) The hybrid substrate of Claim 1 wherein said ~~first~~ bottom semiconductor layer has a (100) crystal orientation and said ~~second~~ top semiconductor layer has a (110) crystal orientation.

Claim 5 (Currently Amended) The hybrid substrate of Claim 1 wherein said ~~first~~ bottom semiconductor layer has a (110) crystal orientation and said ~~second~~ top semiconductor layer has a (100) crystal orientation.

Claim 6 (Currently Amended) The hybrid substrate of Claim 1 wherein said ~~first~~ bottom semiconductor layer comprises a relaxed semiconductor material or a stack of a relaxed semiconductor material and a strained semiconductor material.

Claim 7 (Currently Amended) The hybrid substrate of Claim 1 wherein said ~~second~~ top semiconductor material comprises a relaxed semiconductor material or a stack of a relaxed semiconductor material and a strained semiconductor material.

Claim 8 (Currently Amended) An integrated semiconductor structure comprising:

a hybrid structure comprising a first device region having a first crystallographic orientation and a second device region having a second crystallographic orientation, said first crystallographic orientation is different from said second crystallographic orientation and said first device region is substantially coplanar to said second device region, wherein at least said first device region or said second device region includes an upper semiconductor layer having a thickness from about 200 nm to about 2 μm and an underlying bonding interface that has an oxide thickness of about 10 nm or greater, said

underlying bonding interface vertically separating said upper semiconductor layer from a lower semiconductor layer said upper and lower semiconductor layers having different crystallographic orientations and said bonding interface is absent from the other device region;

an isolation region separating said first device region from said second device region; and

at least one first semiconductor device located in said first device region and at least one second semiconductor device located in said second device region.

Claim 9 (Original) The integrated semiconductor structure of Claim 8 wherein the first crystallographic orientation is (110) and the second crystallographic orientation is (100).

Claim 10 (Original) The integrated semiconductor structure of Claim 9 wherein said at least one first semiconductor device is a pFET and the at least one second semiconductor device is an nFET.

Claim 11 (Original) The integrated semiconductor structure of Claim 8 wherein the first crystallographic orientation is (100) and the second crystallographic orientation is (110).

Claim 12 (Original) The integrated semiconductor structure of Claim 11 wherein said at least one first semiconductor device is an nFET and the at least one second semiconductor device is a pFET.

Claim 13 (Original) The integrated semiconductor structure of Claim 8 wherein the first device region includes a regrown semiconductor material located atop a first

semiconductor material, said regrown semiconductor material having the same crystallographic orientation as the first semiconductor material.

Claim 14 (Original) The integrated semiconductor structure of Claim 13 wherein said regrown semiconductor material is recessed and another semiconductor material is formed atop the recessed regrown semiconductor material.

Claim 15 (Original) The integrated semiconductor structure of Claim 14 wherein said another semiconductor material is a strained semiconductor or a stack comprising a relaxed semiconductor and a strained semiconductor.

Claim 16 (Original) The integrated semiconductor structure of Claim 8 wherein said first and second semiconductor device regions both include strained Si.

Claim 17 (Original) The integrated semiconductor structure of Claim 13 wherein said regrown semiconductor material comprises a strained semiconductor layer located atop a relaxed semiconductor layer.

Claim 18 (Cancelled)